REMARKS

Applicants submitted the above claims in the parent application. The Examiner, however, objected to them as allegedly being directed to an invention that is separate and distinct from the invention originally claimed and examined. Accordingly, he refused to enter these claims.

While Applicants have not formulated an opinion on this objection, Applicants have decided to file this divisional application and amendment to pursue the claims herein.

In order to advance the prosecution of this application, Applicants will address herein each of the Examiner's objections and rejections from the last substantive action in the parent application.

Specification

In response to the Examiner's objection to the specification in the parent application, Applicants are amending the specification herein. This should overcome any objection to the specification.

Claim Rejections - 35 USC §102

In the parent application, the Examiner rejected the independent claims under 35 USC §102(b) as being anticipated by JP 08-055847 (Yamazaki et al.). This rejection is respectfully traversed.

Independent Claim 41 herein states that the semiconductor device comprises a first LDD region in the first semiconductor layer that is not overlapped with the first gate electrode; a second LDD region in the second semiconductor layer that is overlapped with the second gate electrode; and a third LDD region in the third semiconductor layer that is partly overlapped with the third gate electrode. Independent Claims 45,48, 51 and 54 state that the semiconductor device comprises a first LDD region in the first semiconductor layer that is not overlapped with the first gate electrode and a second LDD region in the second semiconductor layer that is overlapped with the second gate electrode.

As these independent claims include the above features (which were not present in the independent claims when they were rejected in the parent application), Applicants respectfully submit that neither structure of these independent claims is disclosed nor suggested by JP 08-055847.

Prior Claim Rejections - 35 USC §103

In the parent application, the Examiner also rejected the dependent claims under 35 USC §103 as being unpatentable over JP 08-055847 in view of JP 10-135468 (Yamazaki et al.). This rejection is also respectfully traversed.

Each of the rejected claims is dependent on the above recited independent claims. Therefore, for at least the reasons explained above for the independent claims, these dependent claims are also patentable over the cited references.

Double Patenting

In the parent application, the Examiner further objected to Claims 76-81 (new Claims 51-56) under 37 CFR 1.75 as being a "verbatim duplicate of claims 70-75 (now Claims 45-50), respectively." Applicants respectfully traverse this objection.

These claims are not "verbatim" duplicates. More specifically, independent Claims 45 and 48 recite for example that the first gate electrode is adjacent to the first semiconductor layer and the second gate electrode is adjacent to the second semiconductor layer. In contrast, Independent Claims 51 and 54 recite that the first gate electrode is over the first semiconductor layer and the second gate electrode is over the second semiconductor layer. Hence, Claims 51 and 54 are related to so-called top gate type semiconductor devices while Claims 45 and 48 are not limited to the top gate type but could also include a bottom gate type, for example. Therefore, the claims are not duplicates.

Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

Please charge our Deposit Account No. 50-1039 for any additional fee due for these new claims and this amendment.

Favorable consideration is earnestly solicited.

Respectfully submitted,

Date: September 24, 2003

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